**CLAIMS**:

1. A field effect transistor comprising:

a semiconductive layer configured to form a channel region;

a pair of spaced conductively doped semiconductive regions in electrical connection with the channel region of the semiconductive layer;

a gate intermediate the semiconductive regions; and

a gate dielectric layer intermediate the semiconductive layer and the gate, the gate dielectric layer being configured to align the gate with the channel region of the semiconductive layer.

2. The field effect transistor according to claim 1 wherein the semiconductive layer comprises a thin film semiconductive layer.

3. The field effect transistor according to claim 1 wherein the gate dielectric layer has a uniform thickness.

4. The field effect transistor according to claim 1 wherein the semiconductive regions are formed over the semiconductive layer.

5. The field effect transistor according to claim 1 wherein the semiconductive regions individually comprise one of a source region and a drain region, and the drain region comprises a field emitter.

6. The field effect transistor according to claim 5 wherein the gate is provided about the field emitter.

7. The field effect transistor according to claim 1 wherein the semiconductive regions individually comprise one of a source region and a drain region, and the drain region comprises a plurality of field emitters.

8. The field effect transistor according to claim 1 further comprising an insulative substrate, and the semiconductive layer is formed over the insulative substrate.

9. The field effect transistor according to claim 8 further comprising a conductive layer intermediate the insulative substrate and the semiconductive layer.

10. The field effect transistor according to claim 1 wherein the gate has an upper outermost surface, and the gate dielectric layer has an upper outermost surface substantially elevationally coincident with the gate upper outermost surface.

11. The field effect transistor according to claim 10 wherein the gate has an upper outermost surface, and the semiconductive regions individually have an upper outermost surface substantially elevationally coincident with the gate upper outermost surface.

12. A field emission apparatus comprising:

a thin film semiconductive layer;

a pair of spaced conductively doped semiconductive regions in electrical connection with the thin film semiconductive layer, at least one semiconductive region comprises a field emitter;

a gate intermediate the semiconductive regions; and

a gate dielectric layer intermediate the thin film semiconductive layer and the gate.

13. The field emission apparatus according to claim 12 wherein the gate is formed about the field emitter.

14. The field emission apparatus according to claim 12 wherein the gate is configured to control current flow intermediate the semiconductive regions and the emission of electrons from the field emitter.

15. The field emission apparatus according to claim 12 wherein the semiconductive regions individually comprise one of a source region and a drain region over the thin film semiconductive layer.

16. The field emission apparatus according to claim 12 wherein the thin film semiconductive layer forms a channel region and the gate dielectric layer is configured to align the gate relative to the channel region.

17. The field emission apparatus according to claim 12 wherein the gate has an upper outermost surface, and the gate dielectric layer has an upper outermost surface substantially elevationally coincident with the gate upper outermost surface.

18. A field effect transistor comprising:

source and drain regions having a channel region positioned therebetween;

a gate positioned operatively proximate the channel region, the gate having an upper outermost surface; and

a gate dielectric layer received intermediate the channel region and the gate, the gate dielectric layer having an upper outermost surface substantially elevationally coincident with the gate upper outermost surface.

19. The field effect transistor according to claim 18 further comprising a thin film semiconductive layer intermediate the source and drain regions and configured to form the channel region.

20. The field effect transistor according to claim 19 wherein the source and drain regions are formed over the thin film semiconductive layer.

21. The field effect transistor according to claim 18 wherein the gate dielectric layer is configured to align the gate with the channel region.

22. The field effect transistor according to claim 18 wherein one of the source and drain regions comprises a field emitter.

23. The field effect transistor according to claim 22 wherein the gate is formed about the field emitter.

24. The field effect transistor according to claim 18 wherein one of the source and drain regions comprises a plurality of field emitters.

25. A thin film transistor comprising:

a thin film semiconductive layer;

a pair of spaced conductively doped semiconductive regions in electrical connection with the thin film semiconductive layer;

a self-aligned gate intermediate the semiconductive regions; and

a gate dielectric layer intermediate the thin film semiconductive layer and the gate.

26. The thin film transistor according to claim 25 wherein the semiconductive regions individually comprise one of a source region and a drain region, and the drain region comprises a field emitter.

27. The thin film transistor according to claim 25 wherein the gate has an upper outermost surface, and the gate dielectric layer has an upper outermost surface substantially elevationally coincident with the gate upper outermost surface.

28. A field emission apparatus comprising:

an insulative substrate;

a conductive layer over the insulative substrate;

a thin film semiconductive layer over the insulative substrate and the conductive layer;

a plurality of semiconductive regions formed over and in electrical connection with the thin film semiconductive layer, the semiconductive regions individually including one of a source region and drain region, the drain region being formed as a field emitter and the thin film semiconductive layer comprising a channel region intermediate the source region and the drain region, the source region and drain region individually include an upper outermost surface;

a gate positioned operatively proximate and self-aligned relative to the channel region, the gate being provided about the field emitter and having an upper outermost surface;

a gate dielectric layer intermediate the gate and the thin film semiconductive layer, the gate dielectric layer having an upper outermost surface substantially elevationally coincident with the source region upper outermost surface, drain region upper outermost surface and gate upper outermost surface, the gate dielectric layer further having a uniform thickness to align the gate relative to the channel region; and

a plurality of conductors individually coupled with one of the gate, the drain region and the source region.

29. A method of forming a field effect transistor comprising:

forming a semiconductive layer having a channel region;

forming plural spaced conductively doped semiconductive regions electrically coupled with the semiconductive layer;

forming a gate dielectric layer over the semiconductive layer;

forming a gate over the gate dielectric layer; and

aligning the gate with the channel region using the gate dielectric layer.

30. The method according to claim 29 wherein the forming the semiconductive layer comprises forming a thin film semiconductive layer.

31. The method according to claim 29 wherein the forming and the aligning of the gate comprise forming a gate layer over the gate dielectric layer and removing portions of the gate dielectric layer and the gate layer.

32. The method according to claim 31 wherein the removing portions of the gate dielectric layer and the gate layer occur in a common processing step.

33. The method according to claim 31 wherein the removing comprises chemical-mechanical polishing.

34. The method according to claim 31 wherein the removing comprises initially removing respective uppermost surfaces of the semiconductive regions before removing any gate material above the gate.

35. The method according to claim 31 wherein the removing provides the gate dielectric layer with an upper outermost surface substantially elevationally coincident with an upper outermost surface of the gate.

36. The method according to claim 29 wherein the forming the gate comprises forming without using any mask.

37. The method according to claim 29 wherein the forming the gate comprises depositing gate material over the gate dielectric layer, and removing portions of the gate material without using a mask over the gate during the removing.

38. The method according to claim 29 wherein the forming the semiconductive regions comprises forming source and drain regions over the semiconductive layer.

39. The method according to claim 29 wherein the forming the semiconductive regions comprises forming a drain region comprising a field emitter.

40. The method according to claim 29 wherein the forming the semiconductive regions comprises forming a drain region comprising a plurality of field emitters.

41. A method of forming a field effect transistor comprising:

providing a semiconductive layer;

forming plural semiconductive regions electrically coupled with the semiconductive layer;

forming a gate dielectric layer over the semiconductive layer; and

forming a gate of gate material over the gate dielectric layer without the use of a mask over the gate material.

42. The method according to claim 41 further comprising aligning the gate with a channel region within the semiconductive layer using the gate dielectric layer.

43. The method according to claim 41 wherein the providing the semiconductive layer comprises forming a thin film semiconductive layer.

44. The method according to claim 41 wherein the forming the gate comprises removing portions of the gate dielectric layer and a gate layer in a common step.

45. The method according to claim 44 wherein the removing self-aligns the gate with a channel region within the semiconductive layer.

46. The method according to claim 44 wherein the removing comprises chemical-mechanical polishing.

47. The method according to claim 44 wherein the removing provides the gate dielectric layer with an upper outermost surface substantially elevationally coincident with an upper outermost surface of the gate.

48. The method according to claim 44 wherein the removing comprises initially removing respective uppermost surfaces of the semiconductive regions before removing any gate material above the gate.

49. The method according to claim 44 wherein the forming the semiconductive regions comprises forming a drain region comprising a field emitter.

50. The method according to claim 44 wherein the forming the semiconductive regions comprises forming a drain region comprising a plurality of field emitters.

51. A method of forming a field effect transistor comprising:

providing a semiconductive layer having a channel region;

providing plural semiconductive regions electrically coupled with the channel region;

forming a gate dielectric layer over the semiconductive layer; and

forming a gate of gate material comprising:

depositing the gate material over the gate dielectric layer;

removing portions of the gate material without using a mask over the gate during the removing.

52. The method according to claim 51 further comprising aligning the gate with the channel region using the gate dielectric layer.

53. The method according to claim 51 wherein the providing the semiconductive layer comprises forming a thin film semiconductive layer.

54. The method according to claim 51 wherein the removing comprises removing portions of the gate dielectric layer and the gate material in a common step.

55. The method according to claim 51 wherein the removing comprises chemical-mechanical polishing.

56. The method according to claim 51 wherein the removing provides the gate dielectric layer with an upper outermost surface substantially elevationally coincident with an upper outermost surface of the gate.

57. The method according to claim 51 wherein the removing comprises initially removing respective uppermost surfaces of the semiconductive regions before removing any gate material above the gate.

58. The method according to claim 51 wherein the providing the semiconductive regions comprises forming a drain region comprising a field emitter.

59. The method according to claim 51 wherein the providing the semiconductive regions comprises forming a drain region comprising a plurality of field emitters.

60. A method of forming a thin film transistor comprising:

forming a thin film semiconductive layer having a channel region;

providing plural semiconductive regions electrically coupled with the channel region;

forming a gate dielectric layer over the thin film semiconductive layer;

forming a gate layer over the gate dielectric layer; and

removing portions of the gate dielectric layer and the gate layer providing a gate self-aligned with the channel region.

61. The method according to claim 60 wherein the providing the semiconductive regions comprises forming a drain region comprising a field emitter.

62. The method according to claim 61 wherein the forming the gate layer comprises forming the gate layer about the field emitter.

63. The method according to claim 60 wherein the removing comprises chemical-mechanical polishing.

64. The method according to claim 60 wherein the removing provides the gate dielectric layer with an upper outermost surface substantially elevationally coincident with an upper outermost surface of the gate.

65. The method according to claim 60 wherein the removing comprises initially removing respective uppermost surfaces of the semiconductive regions before removing any gate material above the gate.

66. A method of forming a thin film transistor comprising:

forming source and drain regions having a thin film channel region positioned therebetween;

forming a gate layer and a gate dielectric layer over the thin film channel region; and

polishing the gate layer to form an isolated gate intermediate the source and drain regions over the thin film channel region.

67. The method according to claim 66 wherein the forming the gate layer comprises forming the gate layer over the source and drain regions.

68. The method according to claim 66 further comprising aligning the gate using the gate dielectric layer.

69. The method according to claim 66 wherein the forming the source and drain regions comprises forming the drain region as a field emitter.

70. The method according to claim 66 wherein the polishing comprises chemical-mechanical polishing.

71. The method according to claim 66 wherein the polishing provides the gate dielectric layer with an upper outermost surface substantially elevationally coincident with an upper outermost surface of the gate.

72. The method according to claim 66 wherein the polishing comprises polishing the gate dielectric layer.

73. The method according to claim 66 wherein the polishing comprises initially polishing respective uppermost surfaces of the source and drain regions before polishing any portions of the gate layer above the gate.